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09/924,185	08/02/2001	Michael Holtzman	M-10246 US	2657

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EXAMINER

CLEARY, THOMAS J

ART UNIT

PAPER NUMBER

2111

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

## Office Action Summary

Application No.

09/924,185

Applicant(s)

HOLTZMAN ET AL.

Examiner

Thomas J. Cleary

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 3-11 and 15-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 3-11 and 15-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>20061025</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 3, 10, 11, 15, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over European Patent Application Publication Number 0 292 248 to Steiner et al. ("Steiner"), US Patent Number 5,544,356 to Robinson et al. ("Robinson"), and knowledge commonly known in the art, as evidenced by US Patent Number 6,088,761 to Aybay ("Aybay"), US Patent Number 6,191,663 to Hannah ("Hannah"), and US Patent Number 4,882,554 to Akaba et al. ("Akaba").

3. In reference to Claims 3 and 10, Steiner discloses an add-on card (See Figure 1 Number 3) for detachably coupling to a processing system (See Figure 1 Number 1) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 1 Number 5); a program storage memory storing at least one operating sequence (See Figure 1 Number 7); a mass storage memory including a portion for storing user data (See Figure 1 Number 9)

and a program memory portion storing at least one additional operating sequence (See Figure 1 Number 8); a processing unit coupled to said interface, said program storage memory, and said mass storage memory (See Figure 1 Number 4), whereby the processing unit can operate on user data transferred between the mass storage memory and the processing system through the interface according to said at least one additional operating sequence (See Column 4 Lines 3-8), and a mass storage interface by which the mass storage memory is connected to a bus (See Figure 1). Steiner further discloses a bus system interconnecting the components of the card, but does not disclose a single bus to which the processing unit, the interface, and the program storage memory are connected. Official Notice is taken that it is well known in the art to interconnect elements of a computing system, such as processors, memories, and interfaces, using a single bus (a multidrop bus), as evidenced by Aybay (See Figure 1), Hannah (See Figures 4 and 13 and Column 2 Lines 8-18), and Akaba (See Figure 1 and Column 1 Lines 16-36). Steiner further does not explicitly disclose the mass storage interface is a non-linear interface, as in Claim 3, or that the mass storage memory is a flash memory, as in Claim 10. However, Steiner does disclose that the mass storage memory may be E<sup>2</sup>PROM or any other appropriate non-volatile Read/Write memory (See Column 2 Lines 21-23 and 51-54). Robinson teaches the use of a flash memory, which is a non-linearly accessed memory, in place of an E<sup>2</sup>PROM as a mass memory device for storing multiple different operating sequences and user data (See Column 6 Lines 7-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Steiner using a multidrop bus as the interconnect between elements and using a flash memory as the mass memory, resulting in the invention of Claim 3, in order to reduce the cost and complexity of the interconnect (See Column 2 Lines 8-18 of Hannah), to reduce the cost and complexity of the processor, since fewer I/O pins are required, and because flash memories achieve much higher densities than E<sup>2</sup>PROMs (See Column 6 Lines 32-40 of Robinson).

4. In reference to Claim 11, Steiner and Robinson teach the limitations as applied to Claim 3 above. Steiner further discloses that the mass storage memory further includes a portion storing system data, whereby the processing unit can operate on data transferred between the card and the unit using the system data (See Figure 1 Number 7).

5. Claims 15 and 25 recite limitations that are substantially equivalent to those of Claims 3 and 10 and are rejected under similar reasoning.

6. In reference to Claim 16, Steiner and Robinson teach the limitations as applied to Claim 15 above. Steiner further discloses that the mass storage memory includes a program memory portion storing at least one additional operating sequence (See Figure 1 Number 8).

7. Claims 4, 8, 17, 19, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, and knowledge commonly known in the art as applied to Claims 3 and 15 above, and further in view of US Patent Number 6,409,089 to Eskicioglu ("Eskicioglu").

8. In reference to Claims 4 and 8, Steiner and Robinson teach the limitations as applied to Claim 3 above. Steiner and Robinson do not teach that the data transferred between the card and the processing system is continuous media, as in Claim 4, and that the at least one additional operating sequence includes a data encryption/decryption routine, as in Claim 8. Steiner does teach that the device is a smart card (See Column 1 Lines 12-26). Eskicioglu teaches a smart card that receives an audio/video stream, which is continuous media, and performing encryption and decryption on the received audio/video stream (See Figure 2 and Column 1 Lines 51-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Eskicioglu using the smart card of Steiner as modified by Robinson and knowledge commonly known in the art, resulting in the inventions of Claims 4 and 8, in order to allow the application programs to be downloaded, debugged, and tested before permanently fixing it to the smart card (See Column 1 Lines 27-30 and Column 4 Lines 12-21 of Steiner), which thus reduces development and production costs.

9. Claims 17 and 23 recite limitations that are substantially equivalent to those of Claims 4 and 8 and are rejected under similar reasoning.

10. In reference to Claim 19, Steiner, Robinson, and Eskicioglu teach the limitations as applied to Claim 17 above. Steiner further discloses that a portion of the mass storage memory contains data prerecorded by the card supplier (See Column 4 Lines 1-21).

11. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, knowledge commonly known in the art, and Eskicioglu as applied to Claims 4 and 17 above, and further in view of US Patent Number 5,418,752 to Harari et al. ("Harari").

12. In reference to Claim 5, Steiner, Robinson, and Eskicioglu teach the limitations as applied to Claim 4 above. Steiner, Robinson, and Eskicioglu do not teach a data cache memory connected to the processor and the mass storage memory for buffering the continuous media transferred between the card and the processing system. Harari teaches the use of a data cache memory for buffering data to be transferred to a flash memory (See Abstract and Column 2 Lines 44-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Eskicioglu, as modified by Steiner,

Robinson, and knowledge commonly known in the art, with the data cache buffer of Harari, resulting in the invention of Claim 5, in order to minimize the number of writes to the flash memory, and thus retard its aging by subjecting it to fewer stress inducing write/erase cycles (See Column 2 Lines 44-48 of Harari); and to increase the write throughput (See Column 2 Lines 54-56 of Harari).

13. In reference to Claim 18, Steiner, Robinson, and Eskicioglu teach the limitations as applied to Claim 4 above. Steiner, Robinson, and Eskicioglu do not teach a data cache memory connected to the processor and the mass storage memory for buffering the continuous media transferred between the card and the processing system. Harari teaches the use of a data cache memory for buffering data to be transferred to a flash memory (See Abstract and Column 2 Lines 44-56). Robinson teaches the use of a flash memory, which is a non-linearly accessed memory, and thus the transferred data is stored non-linearly (See Column 6 Lines 7-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Eskicioglu, as modified by Steiner, Robinson, and knowledge commonly known in the art, with the data cache buffer of Harari, resulting in the invention of Claim 5, in order to minimize the number of writes to the flash memory, and thus retard its aging by subjecting it to fewer stress inducing write/erase cycles (See Column 2 Lines 44-48 of Harari); and to increase the write throughput (See Column 2 Lines 54-56 of Harari).



14. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, and knowledge commonly known in the art as applied to Claim 3 and above, and further in view of US Patent Number 6,266,671 to Niimura ("Niimura").

15. In reference to Claims 6 and 7, Steiner and Robinson teach the limitations as applied to Claim 3 above. Steiner and Robinson do not teach that said at least one operation sequence includes a decompression program, as in Claim 6, or a compression program, as in Claim 7. Niimura teaches a card device having a memory which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Steiner, as modified by Robinson and knowledge commonly known in the art, with the data compression and decompression ability of Niimura, resulting in the invention of Claims 6 and 7, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

16. Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, and knowledge commonly known in the art as applied to Claims 3 and 15 above, and further in view of US Patent Number 5,987,155 to Dunn et al. ("Dunn").

17. In reference to Claim 9, Steiner and Robinson teach the limitations as applied to Claim 3 above. Steiner and Robinson do not teach that at least one additional operating sequence includes a voice-recognition program. Dunn teaches a smart card which receives voice recognition information from the host for processing (See Column 6 Lines 8-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the voice-recognition smart card of Dunn using the smart card of Steiner as modified by Robinson and knowledge commonly known in the art, resulting in the invention of Claim 9, in order to allow the application programs to be downloaded, debugged, and tested before permanently fixing it to the smart card (See Column 1 Lines 27-30 and Column 4 Lines 12-21 of Steiner), which thus reduces development and production costs.

18. Claim 24 recites limitations that are substantially equivalent to those of Claims 9 and is rejected under similar reasoning.

19. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, knowledge commonly known in the art, and Eskicioglu, as applied to Claim 17 and above, and further in view of Niimura.

20. In reference to Claims 20 and 21, Steiner, Robinson, and Eskicioglu teach the limitations as applied to Claim 17 above. Steiner, Robinson, and Eskicioglu do not teach that said at least one operation sequence includes a decompression program, as in Claim 20, or a compression program, as in Claim 21. Niimura teaches a card device having a memory which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Eskicioglu, as modified by Steiner, Robinson, and knowledge commonly known in the art, with the data compression and decompression ability of Niimura, resulting in the invention of Claims 20 and 21, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

21. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Steiner, Robinson, and knowledge commonly known in the art as applied to Claim 15 above, and further in view of US Patent Number 5,995,018 to Hane et al. ("Hane").

22. In reference to Claim 22, Steiner and Robinson teach the limitations as applied to Claim 15 above. Steiner and Robinson do not teach that the data transferred between the interface and the mass storage memory is a navigation database. Hane teaches a

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smart card for receiving, storing, and transmitting a navigation database (See Column 8 Lines 35-44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the smart card having a navigation database of Hane using the smart card of Steiner as modified by Robinson and knowledge commonly known in the art, resulting in the invention of Claim 22, in order to allow the application programs to be downloaded, debugged, and tested before permanently fixing it to the smart card (See Column 1 Lines 27-30 and Column 4 Lines 12-21 of Steiner), which thus reduces development and production costs.

### ***Specification***

23. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code (See Page 3 Paragraph 9). Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

### ***Response to Arguments***

24. Applicant's arguments filed 25 October 2006 have been fully considered but they are not persuasive.

25. Applicant has argued that the memory of Steiner is not a mass storage memory, as the combined memory size of Steiner is only 7k Bytes (See Page 6 Paragraph 4 and Page 7 Paragraph 2). In response, the Examiner notes that this memory size was given as an example memory size and is not limited as such (See Column 3 Lines 56-59). Because the memory size can be varied, Steiner anticipates the use of a mass-storage memory as the memory.

26. Applicant has argued that the data storage area is not for user data (See Page 7 Paragraph 1 and Page 8 Paragraph 3). In response, the Examiner notes that Applicant has not given any specific definition as to what types of data comprise user data. Thus, given the broadest reasonable interpretation, data relevant to the intended use of the card is user data. Further, as the user of the card chooses what data is to be stored in the data storage area, this data is general data of the users choosing.

27. Applicant has argued that Steiner does not teach a memory interface, nor does it teach, suggest, or support a non-linear interface (See Page 7 Paragraph 1 and Page 8 Paragraph 3). In response the Examiner notes that a memory interface is an inherent part of the memory that allows the memory to communicate with the bus and the microprocessor, as an interface, by definition, is the point at which a connection is made between two elements so that they can work together (See 'interface' in The Microsoft Press Computer Dictionary, 2<sup>nd</sup> Edition). Further the Examiner notes that a linear interface is not required in order to access an application program of operating system

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to be executed. As defined by the Applicant and interpreted by the Examiner, a non-linear interface is a non-random interface in which "the contents...can not be addressed randomly...or, more accurately, can only be accessible in blocks that are too large for the controller to utilize without first reading out and caching the whole block (See Paragraph 15 of the Specification). As a flash memory stores data in a non-linear fashion and is not randomly accessible, it must inherently include an interface that is non-linear. Thus, using the flash memory of Robinson as the non-volatile memory of Steiner, which can be any appropriate non-volatile memory (See Column 2 Lines 21-23 and 51-54), would necessarily include a non-linear interface.

***Conclusion***

28. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: US Patent Application Publication Number 2003/0018587 to Althoff et al.; US Patent Number 6,532,152 to White et al.; and US Patent Number 6,298,477 to Kessler; which each disclose that smart cards having mass storage memory are well known in the art.

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

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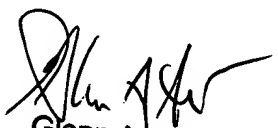
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TJC



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